

What is claimed is:

1. A memory array, comprising:
  - an array plate;
  - a number of memory cells, each cell including:
    - a first source/drain region coupled to the array plate;
    - a second source/drain region;
    - a channel region between the first source/drain region and the second source/drain region;
    - a dielectric layer located over the channel region;
    - a gate electrode located over the dielectric layer;
    - a ferroelectric dielectric coupled to the gate electrode; and
    - a control electrode coupled to the ferroelectric dielectric.
2. The memory array of claim 1, wherein, the ferroelectric dielectric layer is a fraction of area of gate electrode.
3. The memory array of claim 1, wherein the ferroelectric dielectric includes a PZT ferroelectric material.
4. The memory array of claim 1, wherein the control electrode includes a platinum control electrode, and wherein a platinum layer is further located between the gate electrode and the ferroelectric dielectric.
5. The memory array of claim 1, wherein the dielectric layer includes silicon oxide.
6. The memory array of claim 1, wherein the gate electrode includes polycrystalline silicon.

7. A memory device, comprising:
  - an array plate;
  - a number of memory cells, each cell including:
    - a first source/drain region coupled to the array plate;
    - a second source/drain region;
    - a channel region between the first source/drain region and the second source/drain region;
    - a dielectric layer located over the channel region;
    - a gate electrode located over the dielectric layer;
    - a ferroelectric dielectric coupled to the gate electrode;
    - a control electrode coupled to the ferroelectric dielectric; and
  - a sense amplifier circuit coupled to the second source drain regions.
8. The memory device of claim 7, wherein the ferroelectric dielectric includes a PZT ferroelectric material.
9. The memory device of claim 7, wherein the control electrode includes a platinum control electrode, and wherein a platinum layer is further located between the gate electrode and the ferroelectric dielectric.
10. A memory array, comprising:
  - an array plate;
  - a number of memory cells, each cell including:
    - a first source/drain region coupled to the array plate;
    - a second source/drain region;
    - a channel region between the first source/drain region and the second source/drain region; and
    - a gate stack located over the channel region, wherein the gate stack includes two capacitors in series, wherein a first capacitor includes a semiconductor oxide dielectric and a second capacitor includes a ferroelectric dielectric.

11. The memory array of claim 10, wherein the second capacitor includes a first platinum portion and second platinum portion on opposite sides of the ferroelectric dielectric.

12. The memory array of claim 10, wherein the first capacitor includes a first semiconductor portion and a second semiconductor portion on opposite sides of the semiconductor oxide dielectric.

13. The memory array of claim 10, wherein the ferroelectric dielectric includes a PZT ferroelectric material.

14. The memory array of claim 10, wherein the semiconductor oxide dielectric includes silicon oxide.

15. A memory device, comprising:  
an array plate;  
a number of memory cells, each cell including:  
a first source/drain region coupled to the array plate;  
a second source/drain region;  
a channel region between the first source/drain region and the second source/drain region; and  
a gate stack located over the channel region, wherein the gate stack includes two capacitors in series, wherein a first capacitor includes a semiconductor oxide dielectric and a second capacitor includes a ferroelectric dielectric; and  
a sense amplifier circuit coupled to the second source drain regions.

16. The memory device of claim 15, wherein the second capacitor includes a first platinum portion and second platinum portion on opposite sides of the ferroelectric dielectric.

17. The memory device of claim 15, wherein the first capacitor includes a first semiconductor portion and a second semiconductor portion on opposite sides of the semiconductor oxide dielectric.
18. A memory array, comprising:  
an array plate;  
a number of memory cells, each cell including:  
a first source/drain region coupled to the array plate;  
a second source/drain region;  
a channel region between the first source/drain region and the second source/drain region;  
a silicon oxide layer located over the channel region;  
a polysilicon layer located over the silicon oxide layer;  
a ferroelectric dielectric between a first platinum portion and a second platinum portion, wherein the first platinum portion is coupled to the polysilicon layer.
19. The memory array of claim 18, wherein the ferroelectric dielectric includes a PZT ferroelectric material.
20. The memory array of claim 18, wherein the ferroelectric dielectric and the second platinum portion are a fraction of the area of the polysilicon layer.
21. A memory array, comprising:  
an array plate;  
a number of memory cells, each cell including:  
a first source/drain region coupled to the array plate;  
a second source/drain region;  
a channel region between the first source/drain region and the second source/drain region;  
a dielectric layer located over the channel region;

a gate electrode located over the dielectric layer;  
a dipole charge storing means coupled to the gate electrode; and  
a control electrode coupled to the dipole charge storing means.

22. The memory array of claim 21, wherein the dipole charge storing means includes a ferroelectric dielectric material.

23. The memory array of claim 21, wherein the dipole charge storing means includes a PZT ferroelectric material.